7. A tunable voltage isolation ground to ground ESD clamp integrated circuit, the clamp comprising:
a dual-direction silicon controlled rectifier formed from transistors and resistors in a substrate of an integrated circuit between a first ground and a second ground; and
trigger elements formed to provided a trigger current to the dual-direction silicon controlled rectifier when a desired voltage between the first and second grounds is reached.

8. The clamp of claim 7, wherein the trigger elements are formed from at least one or more diodes and a one or more zener diodes.

9. The clamp of claim 7, wherein in the dual-direction silicon controlled rectifier further comprises:
a first silicon controlled rectifier (SCR) including,
a first well of the first conductivity type formed in a second well of the second conductivity type;
a first region of a second conductivity type with high dopant concentration formed in the first well of the first conductivity type, and
a third well of the first conductivity type formed a select distance from the first well of the first conductivity type in the second well of the second conductivity type; and
a second SCR including,
the third well of the first conductivity type,
a second region of the second conductivity type with high dopant concentrations formed in the third well of the first conductivity type, and
the first well of the first conductivity type.

10. The clamp of claim 9, wherein the trigger elements further comprise:
a first overlapping region including first section within the first well having a high dopant concentration of the first type and a second section outside the first well having a high dopant concentration of the second type; and
a second overlapping region including first section within the third well having a high dopant concentration of the first type and a second section outside the third well having a high dopant concentration of the second type.

11. The method of claim 9, wherein spacing of the first and third wells, and regions define at least one of a holding voltage, a dynamic resistance and trigger current.

12. The clamp of claim 9 wherein the dual-direction silicon controlled rectifier further comprises:
a first transistor of a first type;
a second transistor of a second type, the second transistor having an emitter coupled to the first ground and a collector coupled to a base of the first transistor, the second transistor further having a base coupled to the second ground across a first of the trigger elements, the base of the second transistor further coupled to a first emitter of the first transistor; and
a third transistor of the second type, having an emitter coupled to the second ground and a collector coupled to the base of the first transistor, the third transistor further having a base coupled to the first ground across a second of the trigger elements, the base of the third transistor further coupled to a second emitter of the first transistor.

13. The clamp of claim 12, wherein each of the second and third transistors further comprises:
a first well of a first conductivity type formed in a second well of a second conductivity type, wherein the second well is formed in a substrate of the first conductivity type.

14. The clamp of claim 12, further comprising:
a first resistor coupled between the first ground and the base of the second transistor; and
a second resistor coupled between the second ground and the base of the third transistor.

15. An electronic device comprising:
a switching regulator including:
at least one switch,
a regulator including control functions configured to operate the at least one switch,
an inductor coupled between the one switch and an output node,
a feed back loop coupled between the output node and the regulator, wherein the regulator switches the at least one switch at a rate based at least in part on the feedback loop;
a first ground coupled to the control function, and
a second ground coupled to the at least one switch; and
a tunable voltage isolation ground to ground ESD clamp coupled between the first and second grounds, the clamp including,
a dual-direction silicon controlled rectifier (SCR) coupled between the first and second grounds; and
trigger elements coupled between the first and second grounds, the trigger elements configured to provided a trigger current to the dual-direction silicon controlled rectifier when a desired voltage between the first and second grounds is reached.

16. The electronic device of claim 15, wherein the trigger elements of the clamp further comprise at least one of one or more diodes and a one or more zener diodes.

17. The electronic device of claim 15, wherein the dual-direction SCR further comprises:
a first transistor of a first type;
a second transistor of a second type, the second transistor having an emitter coupled to the first ground and a collector coupled to a base of the first transistor, the second transistor further having a base coupled to the second ground across a first of the trigger elements, the base of the second transistor further coupled to a first emitter of the first transistor; and
a third transistor of the second type, having an emitter coupled to the second ground and a collector coupled to the base of the first transistor, the third transistor further having a base coupled to the first ground across a second of the trigger elements, the base of the third transistor further coupled to a second emitter of the first transistor.

18. The electronic device of claim 17, wherein the clamp further comprises:
a first resistor coupled between the first ground and the base of the second transistor; and
a second resistor coupled between the second ground and the base of the third transistor.

19. The electronic device of claim 15, wherein in the dual-direction silicon controlled rectifier of the clamp further comprises:
a first SCR including,
a first well of the first conductivity type formed in a second well of the second conductivity type;
a first region of a second conductivity type with high dopant concentration formed in the first well of the first conductivity type, and